Dkt. 2271/76704

REMARKS

The application has been reviewed in light of the Office Action dated October 31, 2007. Claims 1-22 were pending, with unexamined and non-elected claims 9-22 having been withdrawn by the Patent Office from examination. By this amendment, claim 1 has been amended to clarify the claimed subject matter, new claim 23 has been added, and nonelected and unexamined claims 9-22 have been canceled, without prejudice to applicant's right to pursue the claims in one or more divisional or continuation applications. Accordingly, claims 1-9 and 23 are now pending, with claim 1 being in independent form.

The title was objected to as purportedly not sufficiently descriptive.

By This, Amendment, the title has been amended.

Withdrawal of objection to the title is requested.

Figures 1-3B were objected to.

The replacement sheets of drawings attached hereto as **Exhibit A** include changes to, and replace, Figs. 1-3B of the original sheets of drawings. Figs. 1-3B are now labeled as prior art.

Withdrawal of objection to the drawings is requested.

Claims 1 and 3 were rejected under 35 U.S.C. §102(b) as purportedly anticipated by Hung et al (US 2003/0203575 A1). Claims 2 and 4 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Hung. Claims 5-8 were rejected under 35 U.S.C. §103(a) as purportedly unpatentable over Hung in view of Mehta (U.S. Patent No. 6,282,123).

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claim 1 of the present application is patentable over the cited art, for at least the following reasons.

The present application relates to a semiconductor device that that includes a nonvolatile

memory cell including a selection transistor and a memory transistor with a floating gate but no control gate, and a peripheral circuit transistor (such as a logic circuit). Applicant devised various constitutions of such a semiconductor device wherein writing to the memory transistor may be adequately performed while protecting the peripheral circuit gate oxide film from damage.

In an aspect of the present application (independent claim 1), a semiconductor device comprises a semiconductor substrate and a nonvolatile memory cell that includes a floating gate, a selection gate and a peripheral circuit gate, ***wherein an impurity concentration of the selection gate and the peripheral circuit gate is higher than an impurity concentration of the floating gate.*** Such a constitution enables the charge retaining characteristics of the memory transistor to be improved, and the resistance of the peripheral circuit gate and the selection gate may be adequately lowered so that the processing speed of the peripheral circuit transistor and the selection transistor may be prevented from decreasing.

Hung, as understood by applicant, proposes a single-poly EPROM (erasable programmable read-only memory) having an isolation region disposed in a substrate 100 to define a striped active area, wherein a deep n-well (DNW) formed in the substrate 100 of the memory area I. The deep n-well 106 is formed by implanting n-type dopants. The implantation is performed by implanting PG with a dosage of 10^{14} at about 1.2 MeV and then implanting PH with a dosage of about $1x10^{13}$ at about 700 KeV (see Hung, paragraph [0035]).

Hung also proposes a memory cell with p-well 122 formed by implanting p-type dopants in the deep n-well, thermally driving the dopants and merging together to form the striped p-well 122 (see Hung, paragraph [0043]) followed by an ion implantation of B11 with a dosage of about $10^{13}/cm^2$ in a memory region of the memory cell (see Hung, paragraph [0045]). In addition,

Hung proposes a common source process for memory area a in which a photoresist layer 150 is formed on the substrate 100 and the photoresist layer 150 has a pattern of source regions on both sides of the p-well 122. A pocket implantation is then performed by implanting n-type dopants. The pocket implantation is executed by implanting PH with a dosage of about $5x10^{13}$ ~$1x10^{14}$ /cm^2 at about 50 KeV (see Hung, paragraphs [0049] to [0051]). Hung also proposes n^- lightly doping and p^- lightly doping are performed to form n^- doped regions 132 and p^- doped regions in p-well 104 and n-well respectively. N^+ heavy doping and p^+ heavy doping are performed to form n^+ doped regions 134 and p^+ doped regions in p-well 104 and n-well respectively. The n^+ heavy doping forms sources/drains of NMOS, for forming sources/drains at memory area I (see Hung, paragraphs [0055] to [0056]).

Hung does not disclose or suggest, however, a semiconductor device comprises a semiconductor substrate and a nonvolatile memory cell that includes a floating gate, a selection gate and a peripheral circuit gate, ***wherein an impurity concentration of the selection gate and the peripheral circuit gate is higher than an impurity concentration for the floating gate.***

Mehta, as understood by applicant, proposes a p-type substrate having a background doping concentration of about $1x10^{15}$ – $1x10^{17}$ cm^3 (see Mehta column 5, lines 56-58). Mehta also discuses a second active region 134 in p-type substrate 105 in which doping concentrations of $5x10^{18}$ to $1x10^{21}$ cm^{-3} are suitable (see Mehta column 5, lines 19-22). In addition, Mehta suggests a Large Angle Tilt Implant utilized to form P+ region 155. An implant of boron of about $1x10^{18}$ is suggested.

Mehta does not disclose or suggest, however, a semiconductor device comprising a semiconductor substrate and a nonvolatile memory cell that includes a floating gate, a selection gate and a peripheral circuit gate, ***wherein an impurity concentration of the selection gate and***

the peripheral circuit gate is higher than an impurity concentration for the floating gate.

The cited art simply does not disclose or suggest a semiconductor device comprising a semiconductor device comprises a semiconductor substrate and a nonvolatile memory cell that includes a floating gate, a selection gate and a peripheral circuit gate, ***wherein an impurity concentration of the selection gate and the peripheral circuit gate is higher than an impurity concentration for the floating gate***, as provided by the subject matter of claim 1 of the present application.

Accordingly, for at least the above stated reasons, Applicant respectfully submits independent claim 1, and the claims depending therefrom, are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance, and earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any fees that are required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

Paul Teng, Reg. No. 40,837
Attorney for Applicant
Cooper & Dunham LLP
Tel.: (212) 278-0400

EXHIBIT A

to
AMENDMENT
(Serial No. 10/588,479)